

**32 bit microcontroller**

**HC32L130 / HC32L136 / HC32F030 series clock control module**

**Suitable**

|  |  |
| --- | --- |
| Series | Product number |
| **HC32L130** | HC32L130E8PA  HC32L130F8UA  HC32L130J8TA |
| **HC32L136** | HC32L136J8TA  HC32L136K8TA |
| **HC32F030** | HC32F030E8PA HC32F030F8UA HC32F030F8TA  HC32F030J8TA  HC32F030K8TA |

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1 Summary

This application note focuses on the clock control module of the HC32L130 / HC32L136 / HC32F030 series.

This application note mainly includes：

* Introduction to system clock module
* Switching the clock source
* RCH frequency switching
* Clock frequency division control
* Peripheral clock control

Note：

－ This application note is a supplement to the application of the HC32L130 / HC32L136 / HC32F030 series. It is not a substitute for the user manual. The specific functions and operation of the registers are subject to the user manual.

1 Function introduction

# The clock control module can be configured with different clock sources as the system clock, can be configured with different system clocks, can start or disable the peripheral clock, and the internal clock has a calibration function to ensure high precision.

# Clock control module

## Clock Tree Schematic

The diagram depicts the connection from the clock source to System CLK, HCLK, PCLK, the crossover relationship, and associated configuration registers. Quickly familiarize yourself with the clock control module by referring to the schematic diagram.

Note：

－ **HC32F030** series does not support **LPtimer**、**LPUART** with **RTC**。

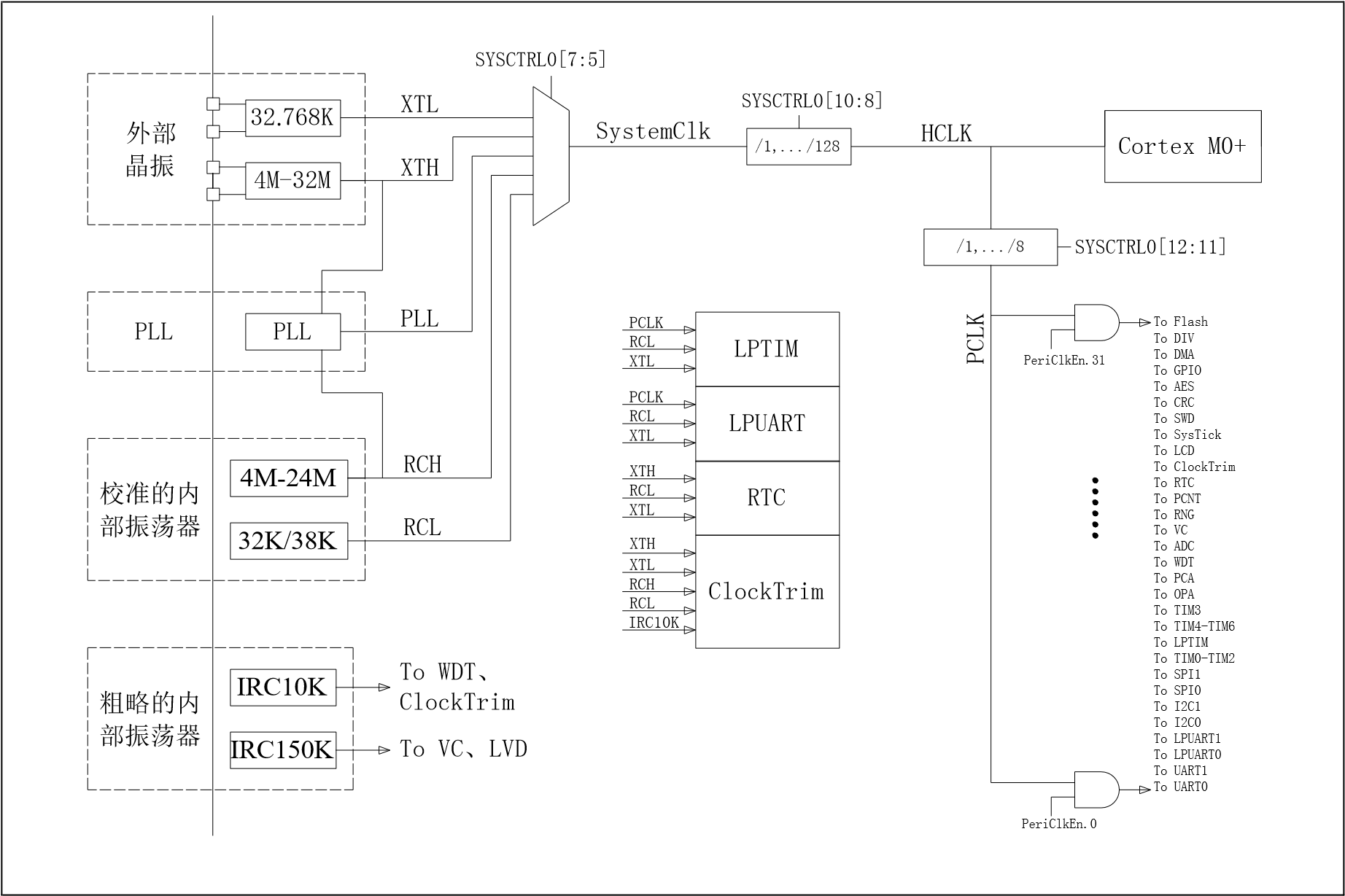


Figure 1. System clock tree

## Introduction to Clock Sources

The clock source is a general term for the MCU internal clock and external clock. This series of chip clock sources includes the following types：

－ System clock

－ External low speed clock (XTL): external 32.768K crystal

－ External high-speed clock (XTH): can be connected to 4M~32M crystal oscillator according to actual needs

－ Internal High Speed RC Clock (RCH): The default system clock for fast system startup and fast wakeup

－ Internal Low Speed RC Clock (RCL): Can be used in low speed, low precision applications with internal phase-locked loop clock (PLL).

－ PLL is optional RCH, XTH as the clock source, support 4M~48M clock output Note: XTL and XTH/PLL can also be configured to be input by external clock source through PC14 and PD00/PD00 ports respectively.

Other clocks:

－ Internal low speed clock (IRC10K): available to WDT and Clock Trim modules

－ Internal low speed clock (IRC150K): for internal debounce, available to VC, LVD modules

## Turning on System Clock Source

The system clock source is opened as follows：

1. Set the stabilization time according to the selected clock：

－ RCL：Configuration RCL\_CR.STARTUP

－ XTH：Configuration XTH\_CR.STARTUP

－ XTL：Configuration XTL\_CR.STARTUP

－ PLL：Configuration PLL\_CR.STARTUP

1. If an external clock is selected, the IO of the corresponding clock is set as the analog input according to the selected clock：

－ XTH: Set PDADS.PD00 and PDADS.PD01

－ XTL：Set PCADS.PC14 and PCADS.PC15

1. If an external clock is selected, the drive capability is set according to the selected clock：

－ XTH: Configuring XTH\_CR.DRIVER

－ XTL: Configuring XTL\_CR.DRIVER

1. If you select the internal clock, you need to load the TRIM value：

－ RCH: Configuration RCH\_CR.TRIM

－ RCL: Configuring RCL\_CR.TRIM

1. If you select the PLL clock, you need to configure the PLL parameters：

－ Input frequency range: Configure PLL\_CR.FRSEL

Multiplier: Configuration PLL\_CR.DIVN Output Frequency Range: Configuration PLL\_CR.FOSC

－ Input Clock Select: Configure PLL\_CR.REFSEL

Note: When selecting the input clock, you must first enable the process configuration according to the system clock source and enable the selected clock source.

1. Enable the selected clock：

－ RCH：Setting SYSCTRL0.RCH\_EN

－ RCL：Setting SYSCTRL0.RCL\_EN

－ XTH：Setting SYSCTRL0.XTH\_EN

－ XTL：Setting SYSCTRL0.XTL\_EN

－ PLL：Setting SYSCTRL0.PLL\_EN

1. Wait for the selected clock source to be stable：

－ RCH：wait RCH\_CR.STABLE

－ RCL：wait RCL\_CR.STABLE

－ XTH：wait XTH\_CR.STABLE

－ XTL：wait XTL\_CR.STABLE

－ PLL：wait PLL\_CR.STABLE

## Switching the clock source

The clock source switching steps are as follows：

1. 1. If the target clock or current clock frequency is higher than 24MHz, set the FLASH read wait period：

－ Setting FLASH\_CR.WAIT

1. Turn on the target clock source (Ref: 3.3 System Clock Source On)
2. Switch the clock：

－ Configuration SYSCTRL0.CLK\_SW5\_SEL；

1. Select whether to turn off other clock sources that are no longer used as needed：

RCH：Clear SYSCTRL0.RCH\_EN

RCL：Clear SYSCTRL0.RCL\_EN

－ XTH：Clear SYSCTRL0.XTH\_EN

－ XTL：Clear SYSCTRL0.XTL\_EN

－ PLL：Clear SYSCTRL0.PLL\_EN

Note：

－ Switching the clock source must note that before the clock is switched, it is necessary to check whether to increase the FLASH read wait period according to the current clock and the target clock maximum frequency value. After the clock switch is successful, the FLASH read wait period can be set or cleared according to the switched clock frequency value.

## RCH Frequency switching

If you need to switch between RCH frequency bands, it is recommended to follow the following process：

1. Switch the system clock source to RCL；
2. Load the update RCH\_CR.TRIM value according to the frequency of the target RCH；
3. Switch the system clock source to RCH.

## Clock Divider Control

In practical applications, any clock source can be selected as the system clock as needed. The system clock is divided to be the CPU operating clock (HCLK), and the HCLK is divided to obtain the peripheral clock (PCLK).

When a clock source is selected as the system clock, a suitable clock can be obtained according to actual needs. The configuration steps of the clock division are as follows:

1. Configure the HCLK division factor：

－ Configuration SYSCTRL0.HCLK\_PRS

1. Configure the PCLK division factor：

－ Configuration SYSCTRL0.PCLK\_PRS

## Peripheral Clock Control

This series of peripheral clock sources has a gate setting. Only when the gate settings are turned on, the corresponding peripherals can be configured and operated. Most peripherals are powered off by default, except that some basic peripherals are turned on by default. Before enabling the peripheral, you need to enable the clock switch of the corresponding peripheral.

To enable the clock of the peripheral module, enable the control bit of the corresponding module of PERI\_CLKEN; turn off the clock of the peripheral module, and clear the control bit of the corresponding module of PERI\_CLKEN.

Note: In the (super) low power mode, the module clock that is not used can be turned off as needed, reducing power consumption.

# Reference examples and drivers

Through the above introduction, with the user manual of HC32L130 / HC32L136 / HC32F030 series, we have this series

MCU's clock control module function and operation method have further mastery.

Huada Semiconductor (HDSC) officially provides the application examples and driver libraries of the module. Users can further familiarize themselves with the application of the module and the driver library by opening the sample project. In actual development, you can also directly refer to the sample. And use the driver library to quickly implement the operation of the module.

* Sample reference：~/HC32L130\_DDL/example/sysctrl
* Driver Library Reference：~/HC32L130\_DDL/driver/…/ sysctrl

# Summary

The above sections briefly introduce the basic functions of the clock control module of the HC32L130 / HC32L136 / HC32F030 series, detailing the functions and operating procedures of the clock module. In the actual application development process, if you need to know more about the usage and operation of the module, you should follow the corresponding user manual. The examples and driver libraries mentioned in this chapter can be used as further experiments and learning by users, or directly in actual development.

# Additional information

Technical support information： [www.hdsc.com.cn](http://www.hdsc.com.cn/)

# Version Information & Contact

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| Date | Version | Modify record |
| 2018/09/03 | Rev1.0 | First release |
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If you have any opinion or suggestions, please feel free to contact us:

during the purchase and use process

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